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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,065	10/30/2003	Michael Anton Barenys	AUS920030682US1	9722

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EXAMINER	
STIGLIC, RYAN M	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 09/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/698,065	BARENYS ET AL.	
	Examiner	Art Unit	
	Ryan M. Stiglic	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *27* is/are allowed.

6)☒ Claim(s) *1-5,8,12-16,19,23 and 24* is/are rejected.

7)☒ Claim(s) *6,7,9-11,17,18,20-22,25 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 are pending and have been examined.

2. Claims 1-5, 8, 12-16, 19, and 23-24 are rejected.

3. Claims 6-7, 9-11, 17-18, 20-22, and 25-26are objected to.

4. Claim 27 is allowed.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 4-5, 8, 12, 14, 16, 19, and 23 rejected under 35 U.S.C. 102(b) as being anticipated by Ying et al. (US006147967A).

Independent claims 1 and 14 recited similar limitations and will be treated as substantially equivalent for the remainder of the office action. Therefore the rejections of claim 1 and its dependents are aptly applied to independent claim 14 and its dependents as shown below.

Regarding claims 1 and 14 Ying discloses,

A device (Fig. 6, 603; col. 10, ll. 10-25) coupled to a serial communications bus (Fig. 6, 641; col. 4, ll. 10-25; col. 14, ll. 10-21), comprising:

- a main section (various components of 603 including CPUs 612 and 622; col. 10, ll. 10-25);

- address logic (col. 9, ll. 16-34);
- switches (Fig. 6, 634 and 642; col. 10, ll. 48-61);
- switch logic for controlling a current position of said switches coupled to said switch logic (col. 11, ll. 36-41);
- said switches being coupled to said communications bus (Fig. 6, 634 and 642; and
- said switches controlling whether said main section, said address logic, said switch logic, or a combination of said main section, address logic, and switch logic is currently coupled to said communications bus (col. 10, ll. 48-61).

Regarding claim 4 Ying discloses,

The device according to claim 1, further comprising: said main section being coupled to said communications bus through said switches (col. 10, ll. 10-25; col. 11, ll. 27-62; col. 14, ll. 10-21).

Regarding claims 5 and 16 Ying discloses,

The device according to claim 1, further comprising: said main section, said address logic, and said switch logic being logically removed from said communications bus when said switches are in a first position (col. 10, ll. 10-25; col. 11, ll. 27-62; col. 14, ll. 10-21).

Regarding claims 8 and 19 Ying discloses,

The device according to claim 1, further comprising: said switches including an input switch device and an output switch device (Fig. 6, 634 and 642; col. 10, ll. 48-61).

Regarding claims 12 and 23 Ying discloses,

The device according to claim 1, further comprising: said address logic for storing an address for said device, said device being addressed on said communications bus utilizing said address (col. 9, ll. 16-34).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2, 3, and 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Ying as applied to claim 1 above, and further in view of Barenys et al. (US 20020108076A1).

Regarding claims 2, 3, and 15 Ying teaches a device attached to a serial bus as recited in claim 1 above. Ying however fails to expressly teach what protocol the communication bus (Fig. 6, 634 and 642) adheres to.

Barenys teach a method for isolating an I^2C bus fault using switching devices dispersed on an I^2C bus. Figure 3 shows an I^2C bus (SCL and SDA) with attached switches (301-304) that effectively isolate I^2C devices (311-314) and other downstream devices [0017;0024;0030-0031]. The I^2C devices contain address logic that maintains a unique address for a given device such

that a particular I^2C device may respond to a master device when its unique address is present on the data lines.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the I^2C bus of the fault isolation system of Barenys as the communication of Ying in order to provide a communication bus that requires wiring and fewer Integrated Circuit connector pins.

9. Claims 13 and 24 are rejected under 35 U.S.C. 103(a) as being obvious over Ying as applied to claim 1 and further in view of Bandholz et al (US 20030212847A1).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the

reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Regarding claims 13 and 24 Ying teaches a device attached to a serial bus as recited in claim 1 above. Ying however fails to expressly teach the address logic contains a hardwired address and an address that overrides a portion of the hardwired address.

Bandholz teach an apparatus for supporting I^2C bus masters on a secondary side of an I^2C multiplexer. Bandholz further teaches that I^2C devices use 7-bit addressing, where four of the 7 bits are hardwired by a manufacturer and the remaining three bits are programmable by the system [0005;0023]. By allowing three bits to be programmed by the system, an I^2C bus is allowed to have $2^3=8$ similar devices on the bus instead of 1 should a hardwired 7-bit code be used.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the hybrid hardwired-programmable I^2C addressing of Bandholz into the fault isolation system of Ying such that the I^2C bus may now support up to 8 similar devices on the bus before requiring a second dedicated bus, thus system operability is expanded.

Allowable Subject Matter

10. Claims 6-7, 9-11, 17-18, 20-22, and 25-26 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claims 6-7, 9-11, 17-18, and 20-22 the Examiner has done a thorough search and found no prior art of record, alone or in combination, that teaches or fairly suggests isolating a main section of an I^2C device while keeping address and switch logic connected to the I^2C bus. Instead, the prior art completely isolates all functionality of and I^2C device. Also the Examiner was unable to find prior art of record, alone or in combination that teaches or fairly suggests either a dual pole switch for use with an I^2C bus that has four separate positions. The Examiner was able to find prior art that teaches or suggests a two-position isolation switch in which the device (behind the switch) is either completely isolated or completely attached to a communication bus. In other words the prior art does not teach or suggest allowing an address and switch logic to be logically attached to the bus while a main section is logically removed from the bus.

With respect to claims 25-26 the Examiner has done a thorough search and found no prior art of record, alone or in combination, that teaches or fairly suggests the limitations of collectively removing all serial devices from the communication bus when it is determined that a plurality of devices are addressed by duplicate addresses. Furthermore the prior art fails to teach or suggest updating the address of at least one of a plurality of devices with duplicate addresses. Likewise

the prior art fails to teach or suggest sending a command to the plurality of devices where the command instructs the devices to reattach to the communications bus.

11. Claim 27 allowed.

The following is an examiner's statement of reasons for allowance: Claim 27 contains limitations.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The various cited pieces of prior art relate to isolating communication bus devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan M. Stiglic whose telephone number is 571.272.3641. The examiner can normally be reached on Monday - Friday (6:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571.272.3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RMS

Paul R. Myers

PAUL R. MYERS
PRIMARY EXAMINER